IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Akhil K. Garlapati et al.		
Title:	VOLTAGE REFERENCE GENERATOR CIRCUIT USING LOW-BETA EFFECT OF A CMOS BIPOLAR TRANSISTOR		
Application No.:	10/813,837	Filed:	March 31, 2004
Examiner:	Rajnikant B. Patel	Group Art Unit:	2838
Atty. Docket No.:	026-0044	Conf. No.:	6047

September 20, 2006

Mail Stop Amendment
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SUMMARY OF APPLICANT-INITIATED INTERVIEW

Applicants appreciate the interview granted between Examiner Easthom and the undersigned on September 20, 2006, during which the finality of the Office action mailed July 17, 2006 was discussed. Examiner Easthom agreed that the finality of the rejection was improper and that the finality of the rejection will be withdrawn.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

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Nicole Teitler Cave _____ Date _____

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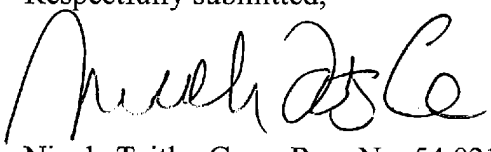
Respectfully submitted,



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